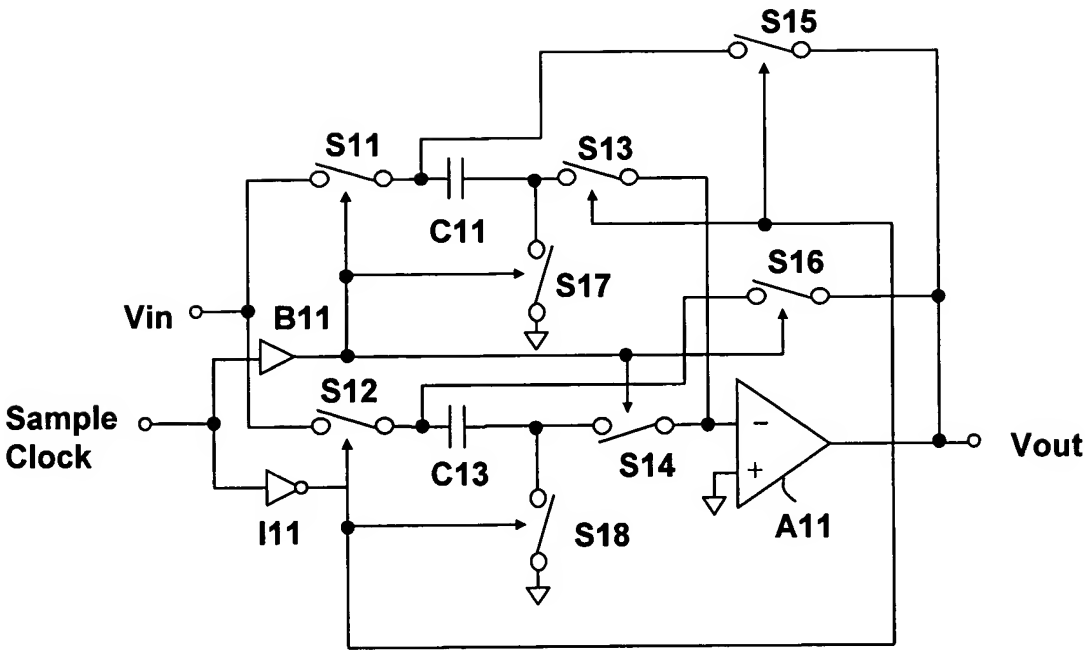
S15
S11
S13
C11
S17
S16
Vin
B11
S12
Sample
Clock
C13
S14
Vout
I11
S18
A11

Fig. 1

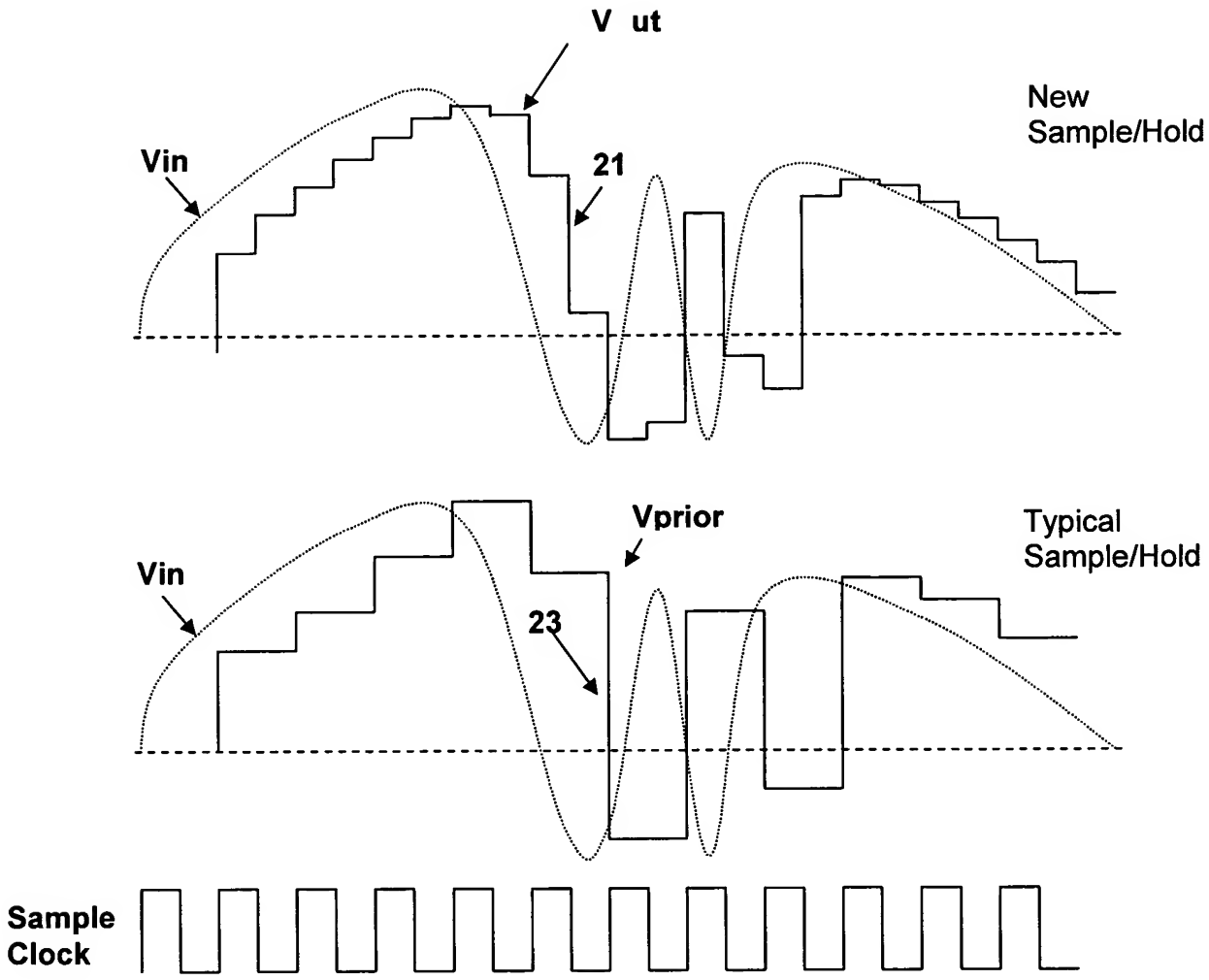
V ut
New
Sample/Hold
Vin
21
Vprior
Typical
Sample/Hold
Vin
23
Sample
Clock

Fig. 2

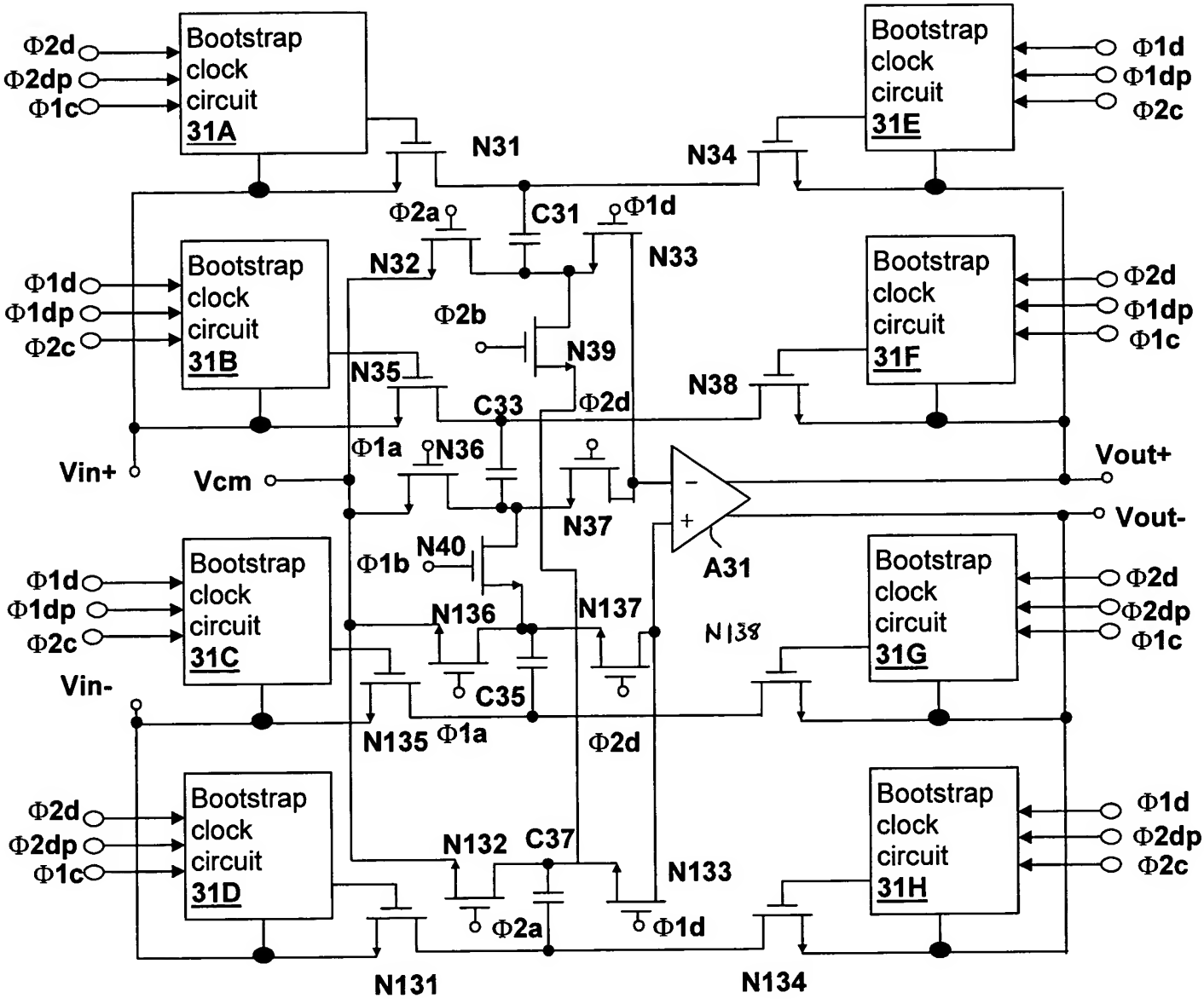
Φ2d
Φ2dp
Φ1c
Bootstrap clock circuit 31A
N31
Φ2a
C31
Φ1d
N33
N32
Bootstrap clock circuit 31E
Φ1d
Φ1dp
Φ2c
N34
Φ1d
Φ1dp
Φ2c
Bootstrap clock circuit 31B
N35
Φ2b
N39
C33
Φ2d
Bootstrap clock circuit 31F
Φ2d
Φ1dp
Φ1c
N38
Vin+
Φ1a
N36
Vcm
N37
Vout+
Vout-
A31
Φ1d
Φ1dp
Φ2c
Bootstrap clock circuit 31C
N40
Φ1b
N136
N137
N138
Bootstrap clock circuit 31G
Φ2d
Φ2dp
Φ1c
Vin-
C35
N135
Φ1a
Φ2d
Φ2d
Φ2dp
Φ1c
Bootstrap clock circuit 31D
N132
C37
N133
Φ2a
Φ1d
Bootstrap clock circuit 31H
Φ1d
Φ2dp
Φ2c
N131
N134

Fig. 3

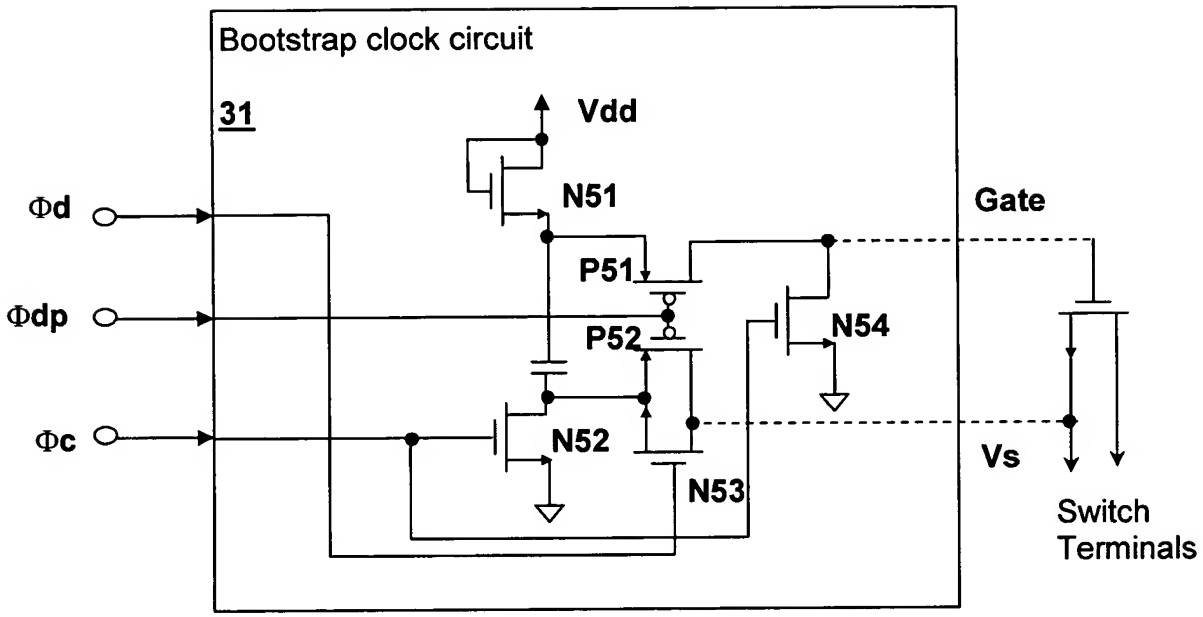
Bootstrap clock circuit
31
Vdd
N51
Gate
Φd
P51
Φdp
P52
N54
Φc
N52
Vs
N53
Switch
Terminals

Fig. 4A

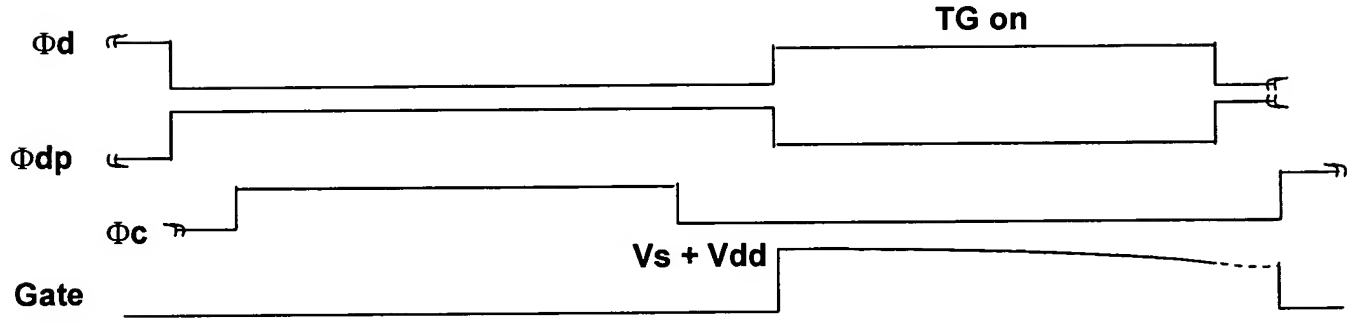
TG on
Φd
Φdp
Φc
Vs + Vdd
Gate

Fig. 4B

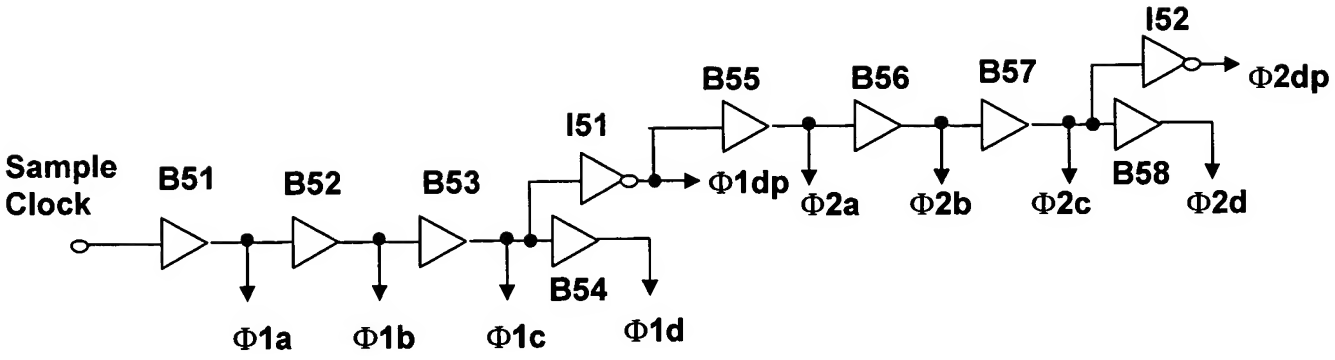
Sample Clock
B51
B52
B53
I51
B54
B55
B56
B57
I52
B58
Φ1a
Φ1b
Φ1c
Φ1d
Φ1dp
Φ2a
Φ2b
Φ2c
Φ2d
Φ2dp

Fig. 5A

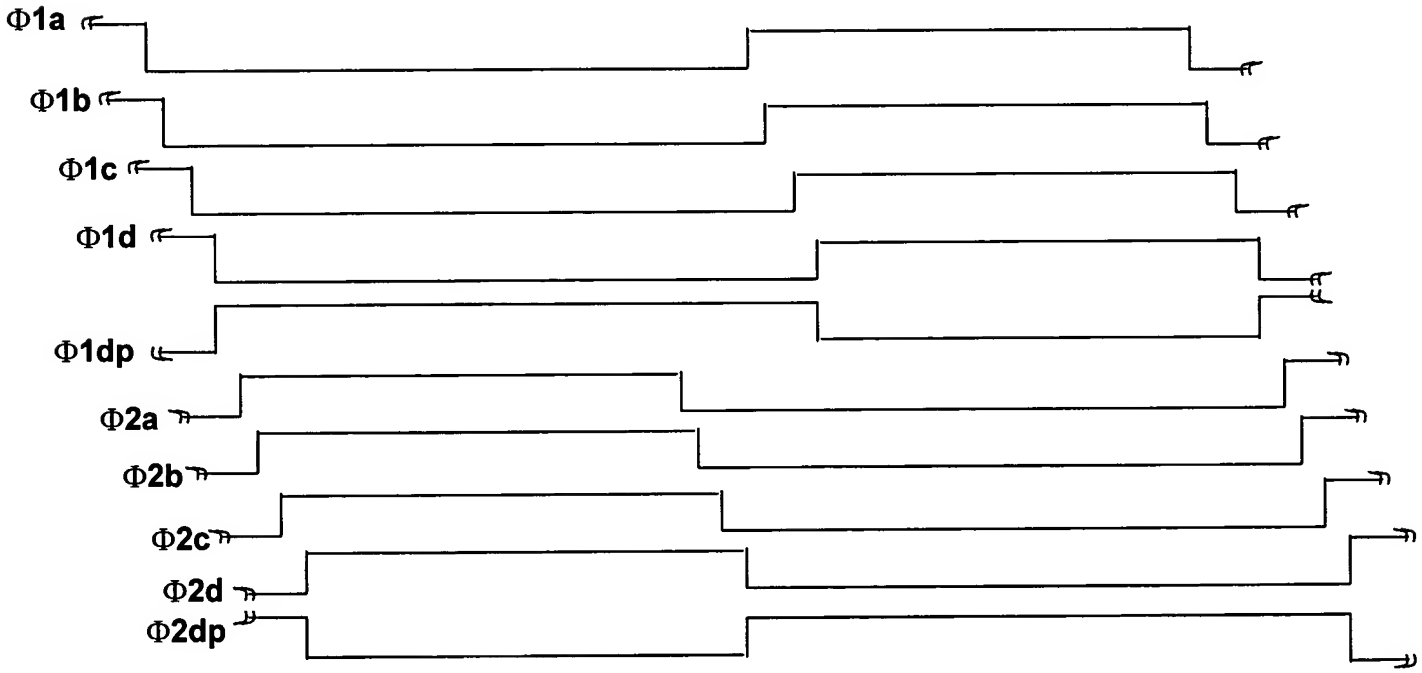
Φ1a
Φ1b
Φ1c
Φ1d
Φ1dp
Φ2a
Φ2b
Φ2c
Φ2d
Φ2dp

Fig. 5B